IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Budong You et al.	Art Unit :	2812
Serial No.	: 10/714,271	Examiner :	Ron Everett Pompey
Filed	: November 13, 2003	Confirmation No.:	2014
		Notice of Allowance Date:	October 5, 2006

Title : A METHOD OF FABRICATING A LATERAL DOUBLE-DIFFUSED MOSFET (LDMOS) TRANSISTOR AND A CONVENTIONAL CMOS TRANSISTOR

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COMMENTS ON EXAMINER'S REASONS FOR ALLOWANCE

Applicant recognizes that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all of the details as to why the claims are allowed. In the above-referenced application, Applicant does not concede that the Examiner's stated reasons for allowance are the only reasons for which the claims are allowable. In particular, Applicant does not concede that all of the identified limitations are necessary to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. Furthermore, the claims may be patentable for other reasons.

Please apply any additional charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12/5/06

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